Dynamic Safe-Area Protection for Power Transistors Employs Peak-Temperature Limiting

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Abstract: *Safe-area protection can be provided for a large power transistor by limiting its peak junction temperature. A pn junction that is distributed throughout the power transistor in close proximity to the entire active emitter makes a satisfactory peak-temperature sensor. Thermal response times under 100 μs are practical, so that dc foldback current limiting is not required. Peak-current limiting and an over voltage shutdown that operates as BV_{CEO} is approached establishes the boundaries of the safe-area curve.*

introduction

Thermal limiting has been employed extensively in power IC's, particularly voltage regulators and power amplifiers [1]–[5]. However, thermal coupling between the sensor and the power transistor has not been good enough that temperature sensing alone could provide adequate protection. Located right at the edge of a power array, a conventional thermal sensor detects only 60-percent of the peak junction-to-case temperature rise; sense delays of milliseconds are also observed. The situation deteriorates rapidly as spacing between the sensor and power element increases to several mils, as is frequently the case. An electrical network that reduces the maximum output current of the power transistor with increasing collector voltage has been used to compensate for inadequate thermal coupling. This foldback current limit should match the safe-area curve for continuous dissipation at the maximum case temperature encountered in practice. At higher temperatures it is expected that the thermal limiting will control the junction temperature.

With a distributed peak-temperature sensor that is tightly coupled to the entire active emitter, foldback current limiting is unnecessary [6]. Maximum capabilities will follow the actual safe-area curve of the power transistor, pulse or continuous, for all operating conditions. The protection is completely effective, even if severe hot spots develop, as long as the current is held below the peak ratings of the transistor and the voltage is less than the collector-emitter sustaining voltage.

Dynamic safe-area protection increases the continuous dissipation ratings that can be guaranteed by an order of magnitude by avoiding arbitrary deratings and the tolerance problems of foldback current limiting. Increased pulse ratings are a bonus. At the same time, much better control of peak junction temperature is maintained under worst-case conditions.

sensor coupling

The effect of thermal sensor placement was evaluated experimentally using the test die sketched in *Figure 1*. The power array was 43 x 5.7 mils with a notch for the first sense emitter. This sense emitter was separated from the active emitters by 4.5 mils on three sides. Temperature within the array was 30°C with 6W dissipation as measured by a separate sense emitter (not shown) immersed within the array. Silicon die thickness was 10 mils. A gold-eutectic die attach to a 13 mil-thick molybdenum interface brazed to a copper heat spreader on a steel T0–3 package completed the thermal system. The plot shows that the temperature rise at the first sensor is little more than half the internal temperature rise and falls off rapidly for more remote sensors.

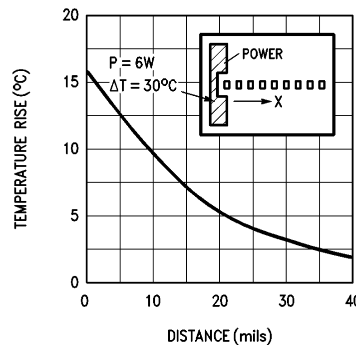

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Figure 1. Thermal sensor temperature rise above case as a function of distance from the power transistor. The power array is 43 x 5.7 mils with a notch for the nearest sensor. The nine sensors are spaced by 5 mils down the centerline. Die size is 61 x 75 mils.

Thermal transient response of this system can be estimated from *Figure 2*. The response of the internal sense emitter might be taken as representative of the peak instantaneous temperature of the active emitters. The adjacent sensor is the first in *Figure 1* while the remote sensor is separated by 20 mils down the centerline from the power array. Millisecond delays in reaching the final temperature are obtained even when the sensor is adjacent to the power source.

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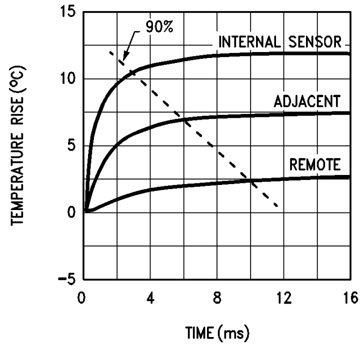

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Figure 2. Transient response of the thermal system sketched in *Figure 1*. The internal sensor is representative of power transistor thermal response. The adjacent sensor has a 3 ms delay in approaching its final temperature. Remote sensor is located 20 mils down the centerline.

Teledeltos resistance paper was used to obtain a two-dimensional solution for the temperature variations within the power array as well as on the outside. The results, plotted in *Figure 3*, assume a uniform heat flux within the power array and a 24 mil equivalent die thickness, corresponding to the hard die-attach method described earlier.

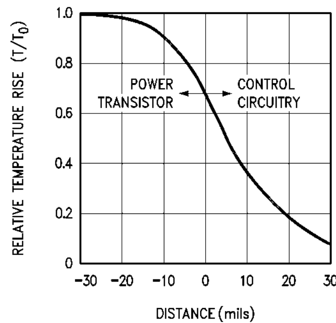

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Figure 3. Surface temperature profile for a two-dimensional IC power transistor as modeled with resistance paper. The curve is scaled to represent a hard die attach to a molybdenum spacer in a copper T0–3 package.

This data suggests that the sensor must be immersed well inside the power array to accurately sense temperature even when ballasting is adequate to maintain uniform conduction throughout. Accounting for three-dimensional effect or the decrease in thermal conductivity of silicon at elevated temperature increases the gradients, as does soft die attach directly to copper [7]. Thermal destabilization as encountered in marginally-ballasted arrays can severely modify results.

Marginal ballasting or die attach voids can cause hot spots that will not necessarily occur at the center of the power array. A single sensor in the center or the array would be an improvement over former methods but will not give the absolute protection of a peak sensor distributed throughout the array.

pn junction sensors

Although not perfect, a pn junction is a satisfactory peak-temperature sensor. The reverse leakage current increases exponentially with temperature, doubling about evey 10°C. Therefore, should a hot spot develop such that only 10-percent of the junction were heated, the peak temperature would have to rise less than 40°C above an uniformly heated junction to give the same leakage current.

The collector current of a transistor also increases exponentially with temperature, with a fixed base-emitter bias, in a manner related to the leakage current. Therefore, if a sense transistor limits temperature at a given emitter-base voltage and collector current, thermal localization will require equally small increases in peak temperature to effect limiting. *Figure 4* plots the temperature error in peak detection as a function of the fraction of the transistor emitter being heated. A nominal limiting temperature of 225°C and a zero emitter-base bias is assumed ($V_{CE} >> 0$). This plot was obtained by solving the V_{BE} equation [8].

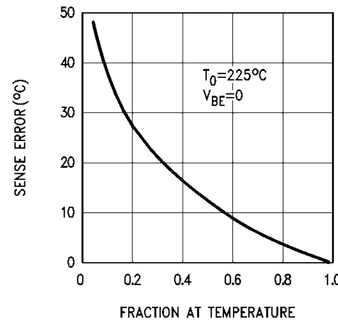

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Figure 4. Temperature increase above 225°C required to maintain constant output from a sense transistor when only a fraction of the emitter area is heated. Zero emitter-base bias is assumed.

An important consideration in dynamic safe-area protection is that the thermal sensor be located close enough to the active emitter that it can control overloads at maximum peak current and operating voltage. Otherwise, a modified foldback current limit would have to be used. Minimum thermal delay also allows the control circuit feedback loop to be frequency compensated so that protection is effected without generating spurious oscillations and interference.

Minimum spacing between the thermal source and the sensor is obtained by putting a sense emitter in the base region of the power transistor located about 0.4 mils from the active emitter. Narrow active emitters are required so that the heat generation cannot electrically or thermally shift away from the sensor. Spacings greater than 0.4 mils were not investigated. However, this spacing does allow for both control-loop stabilization and capture times under 100 μs.

Initially, the leakage current of the sense emitter was used to establish thermal limiting. Unresolved practical problems and the fact that forward-biased emitter-base voltage is far better characterized for temperature sensing shifted emphasis. With proper design, the latter can hold a $\pm$15°C error in limiting temperature over the production distribution, exclusive of severe hot-spot problems. Eliminating control-loop oscillations caused by stray coupling into high-impedance nodes also proved easier.

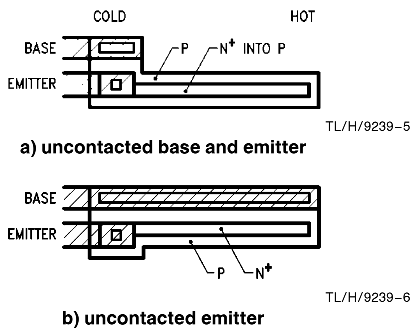
thermoelectric effects

Large IC power transistors have topological design problems caused largely by the topside collector contact. Getting the base lead out of an array is difficult enough. Adding thermal-sense leads is not a welcome challenge. Fortunately the thermal sensor can be operated at low current. In principle, the sensor can be included into the array using doped silicon as a second level conductor. If this is done, thermoelectric potentials can alter the apparent V_{BE} of the sensing transistor.

When a temperature gradient is established along the length of a conductor, carriers will diffuse toward the cold end until an electric field is established that balances the thermal diffusion [9]. The resulting voltage is called the Seebeck voltage and depends on the temperature differential. With most metals, the Seebeck coefficient is in the order of 1 μV/°C. With heavily-doped semiconductors it is about 100 μV/°C, increasing above 1 mV/°C for light doping [9], [10].

A distributed transistor structure that does not require metallization is shown in *Figure 5a*. An emitter stripe is diffused into a base region with contact made only at the cold end. The Seebeck voltages across the length of the base and emitter both increase the apparent V_{BE} at the hot end as measured at the cold end, causing a substantial temperature-sense error.

A second structure is shown in *Figure 5b*. A metal contact is used along the length of the base, but there is none on the emitter. The Seebeck-voltage error is essentially that of the emitter alone. Eliminating the Seebeck voltage of the more-lightly-doped base significantly improves sensor accuracy. As near as can be determined, the temperature-measurement error is about 6-percent of the junction-to-case temperature rise when the cold end is located at the periphery of the power array.



a) uncontacted base and emitter

b) uncontacted emitter

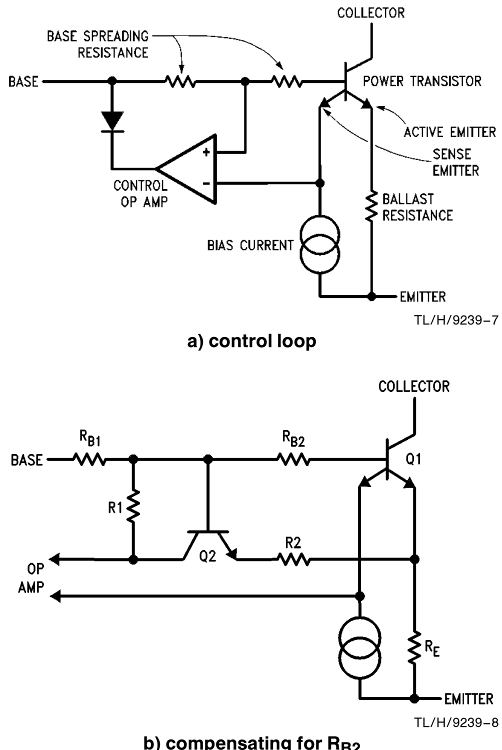
Figure 5. A distributed, peak-temperature-sensing transistor can be formed without continuous metal contacts on the base and emitter as shown here. However, thermoelectric voltages can alter performance.

The sensor in *Figure 5b* does respond to peak temperatures along its length. Further, it can share metallization with the power transistor; so it can be integrated into the power array without requiring additional metal traces. Located in the same base region as the active emitters, sensor coupling can also be optimized as mentioned earlier.

control circuitry

A functional diagram of the control loop for peak-temperature limiting is shown in *Figure 6a*. The sense emitter within the power transistor is forward biased and operated at a current that will give $V_{BE} = 0$ at the desired limiting temperature (about 225°C). Normal transistor operation is obtained at elevated temperatures with zero or even reverse emitter-base bias as long as collector-emitter voltage is above a few-hundred millivolts. The differential inputs of an op amp are connected between the sense emitter and the common base lead for the sense and power transistors. A diode isolates the op amp output from the base circuitry when the sense emitter potential is below that of its base and the op amp output is high. As the V_{BE} of the sense transistor starts to reverse with increasing temperature, the op amp output will drop, taking over control of the base circuitry such as to regulate hot-spot temperature.

Base resistance common to the sense and power transistors is a source of positive feedback in the control loop. This can be minimized by using a separate sense contact to the base near the sense emitter such that the base spreading resistance of the power transistors is shifted outside the input circuitry of the op amp. Any residual common resistance can be compensated for by using the arrangement shown in *Figure 6b*. Changes in voltage across R_{B2} produce similar changes across R_2. The resulting change in R_1 in the collector of Q_2 is of a polarity to cancel the change across R_{B2} as seen at the op amp input. Undercompensation results in oscillation in thermal limiting; overcompensation



a) control loop

b) compensating for R_{B2}

Figure 6. Sense emitter on the power transistor is biased so that $V_{BE} = 0$ at the limiting temperature. At this temperature, the op amp will absorb base drive to regulate temperature. Uncompensated base-spreading resistance can cause positive feedback.

gives a temperature-sense error. Compensation is most important at lower collector voltages for the power transistor because base current in thermal limit will be highest.

Problems with base-spreading resistance as well as thermoelectric potentials can be mitigated by biasing the sense emitter in the reverse (leakage) mode. Even so, forward bias operation appeared to give more satisfactory overall results.

A simplified schematic of an IC control op amp is shown in *Figure 7*. It is designed to operate from the power transistor collector-emitter voltage. Some effort was put into obtaining control-loop stability to avoid the oscillations observed with conventional thermal limit even as controlled by hysteresis. The object was to provide effective protection with a minimum of spurious interference or signal distortion.

The differential input stage of the op amp is formed by lateral PNP transistors Q_3 and Q_4. The collectors of those transistors feed into an inverted transistor current mirror, Q_5 and Q_6, with feedback buffered by Q_7. The mirror output from Q_6 feeds another buffer Q_8, that drives Q_{10}. Additional current gain to take over command of the base drive is provided by Q_{12}.

Minimal operating currents were used for Q_5 and Q_6 so that the control loop could be compensated with a small diffused capacitor, C_1. The resulting high impedance nodes in the current mirror output required the use of inverted transistors so that parasitic capacitances would not cause loop instability in certain applications. Tub leakage currents were also a consideration in using the inverted-transistor configuration.

The peak-current-limit boundary of the safe-area curve is also established by this circuit. The voltage on the base terminal is clamped at 2 V_{BE} plus the drop across R_5. When the drop across the ballast resistance of the modified Darlington power transistor R_1 equals this voltage, Q_{12} will conduct, inhibiting any further increase in current. Although not precise, this current limit is adequate for protecting the bond wires while not restricting the output capabilities of the IC.

maximum temperature

Silicon IC's are generally rated for a maximum junction temperature of 150°C. With linear ICs, this is not an arbitrary limit: most do not function properly above 150°C because of circuit problems unrelated to reliability. Increased leakage currents are a limiting factor with high temperature operation. Further, the V_{BE} of the transistors falls with increasing temperature while the collector-saturation threshold (V_{TH}) rises. If V_{BE} does not exceed V_{TH}, many popular configurations like a current mirror or ΔV_{BE} current source do not operate properly [11]. IC's can be designed to operate above 200°C, but the cost and performance at normal temperatures are usually compromised.

Bipolar power transistors are rated for a junction temperature of 200°C. This is not a fundamental limit. Power transistors can usually be biased such that falling V_{BE} and rising leakage current can be accommodated to temperatures approaching 400°C. Further, no inherent failure mechanism was identified in running hermetically packaged NPN IC transistors at 300°C for 5000 hours with bias. Double-diffused NPνN transistors operate properly at temperatures where the collector region is intrinsic; however, IC Power transistors require a sinker diffusion with the topside collector contact if they are to be operated with an intrinsic collector region.

Because of the substantial temperature gradients normally encountered in power IC's, it is reasonable to establish different maximum temperatures for the power transistor and

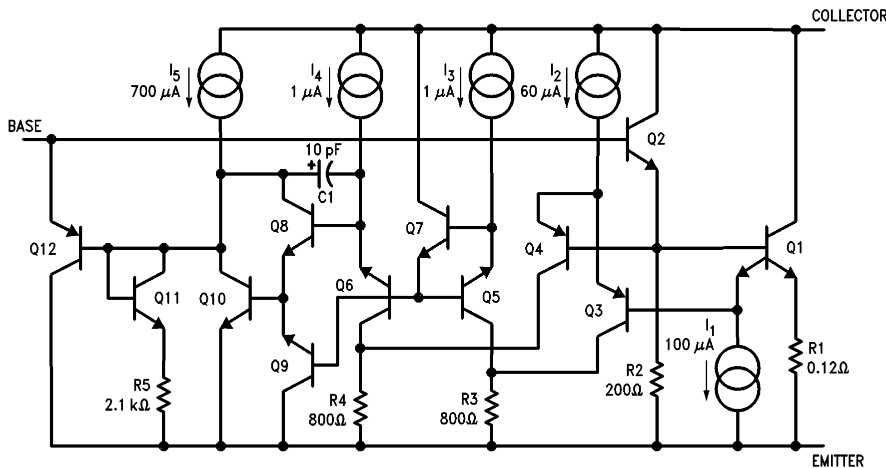


Figure 7. Simplified schematic of the control op amp. Low bias current for current mirror, Q5 and Q6, allow loop compensation with a small capacitor, C_1. Inverted transistors are used to minimize parasitic leakage and capacitance to substrate.

low-level circuitry. Implementing this requires separate temperature controllers, because the package temperature can approach that of the power transistor when minimal heat sinking is used. Excessive temperature in the low-level circuitry could make the temperature limiting malfunction. A peak temperature limit of 250°C for the power transistor and 150°C for the low-level circuitry has proven satisfactory for IC's in hermetic metal cans.

power cycling

If the thermal-expansion coefficient of a power package is substantially different from that of silicon, power cycling will cause mechanical stress. For example, if a large silicon die is rigidly mounted to copper, the stress can cause the die to crack. This can be avoided by using a soft-solder die attach that has some give. However, soft die attach fatigues with cycling [12]. Failures beginning at 3×10^3 cycles with a 70°C junction-to-case temperature rise are not uncommon.

Molybdenum has nearly the same expansion coefficient as silicon. It can be used as an interface between the silicon and copper to equalize stress, so that a hard, gold-eutectic die attach can be used. This system is virtually immune to thermal fatigue.

Metallization failures unrelated to electromigration can be induced by rapid temperature cycling [13]. With copper-doped aluminum passivated with phosphorosilicate glass, failures have been induced in a power array at 10^6 cycles with a temperature rise of 175°C in a millisecond. Reducing the rate of temperature rise mitigates the problem. Degradation begins with cracks in the passivating layer that can be observed optically. Next, metal oozes through the cracks. Ultimately, failure occurred from shorting between the emitter and base metallization of the power transistor.

overvoltage shutdown

Although bipolar transistors can be operated above BV_{CEO}, it is rarely practical to do this with a conducting power transistor. Protecting a circuit from excessive voltage is best done by shutting it down as BV_{CEO} is approached so that it can stand off voltages equal to BV_{CER}. Since production variations in BV_{CEO} can be substantial, it is desireable that shutdown be activated at a voltage directly related to the capabilities of the IC power transistors.

The open base breakdown of a transistor is related to current gain. It has a negative resistance characteristic because it is activated by leakage currents where gain is low, falling to a lower voltage where gain peaks. Because of this, an open base transistor will not break down until its voltage is above the minimum BV_{CEO}.

The circuit shown in *Figure 8* avoids this problem by operating the voltage sensor, Q_1, near its current-gain peak. Key to its operation is the pinched-base resistor, R_1. With modern processing of double-diffused NPN transistors the sheet resistance of a pinch resistor is given by $R_{\square} = 30\ h_{fe}$*, where h_{fe} is the peak ac current gain at $V_{CB} = 0$. The equation is reasonably valid over a −55°C to +150°C temperature range.

*Although this has not been established theoretically, there is considerable experimental evidence showing correlation between h_{fe} and pinched-base sheet resistivity within ±30-percent over a wide range of processing variables.

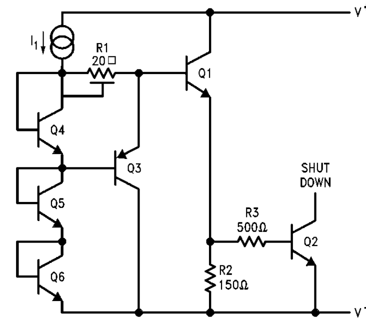


Figure 8. This overvoltage detector gives a shutdown signal as the BV_{CEO} of Q_1 is approached based upon the increase in h_{fe} with voltage. The value of R_1, a pinched-base resistor, is proportional to the h_{fe} at low voltage.

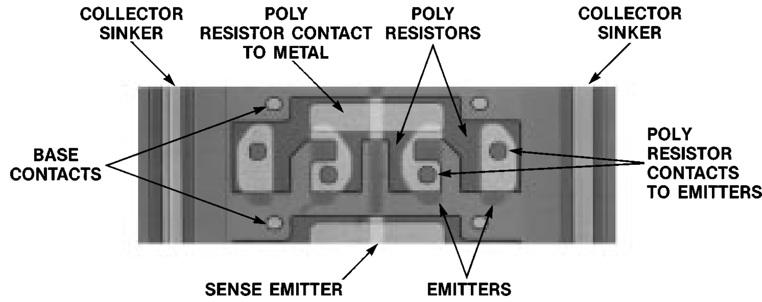
Given this relationship, the pinch resistor in the base of Q_1 in *Figure 8* can be translated to an emitter resistor having a sheet resistance of 30Ω/□, independent of h_{fe} and temperature. Thus, the bias on the base of Q_2 will be 0.2 V_{BE} with low collector voltage on Q_1, rising to V_{BE} as the h_{fe} of Q_1 increases to five-times its low voltage value. This occurs at approximately 0.95 BV_{CEO}. With a supply voltage greater than BV_{CEO}, Q_3 clamps the base of Q_1, absorbing reverse base current, there by limiting its emitter current to a safe value. The output of Q_2 can be used to shut down the IC.

results

This work was done as part of the development of a monolithic IC op amp [6]. The device, as completed, is rated to deliver ±10A, or 150W into a 4Ω load. This performance represents a dramatic increase over what has been accomplished using older techniques. When worst-case specifications and the added stresses imposed by reactive loads are taken into account, the practical value of dynamic safe-area protection becomes even more obvious.

The data presented here is from an IC power-transistor design using the basic cell structure shown in *Figure 9*. There are four power emitters per cell, each individually ballasted with a polycrystalline-film resistor. The cell is bisected by a thermal-sense emitter that is spaced 0.4 mils from the closest power emitter. The complete power transistor is composed of fifteen cells stacked in columns, with nine columns in the array. The safe area curve of the power transistor is nominally bounded by a peak-current limit of 12A and a voltage shutdown at 85V. The thermal resistance for continuous dissipation at 20V is 2.2°C/W.

The pulse power ratings obtained with dynamic safe-area protection are given in *Figure 10*. The pulse capability far exceeds that obtained by earlier methods using gradient-controlled current limiting [4], [5]. With sine-wave drive to reactive loads, peak power can exceed four times average. This power peak has a constant-power-pulse equivalent of about one-fifth the waveform period. Potential improvements in power capability should be clear.



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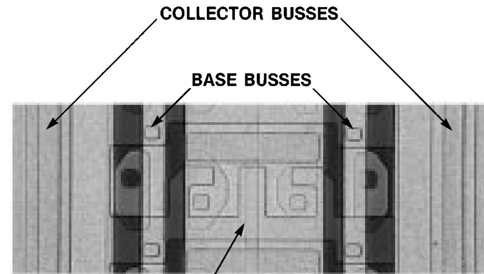
a) before metallization



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b) after metal etch

Figure 9. Photomicrograph of the power-transistor cells used in this study. Each emitter is ballasted with a polycrystalline-film resistor. The thermal-sense emitter bisects the cell. Cells are stacked into vertical columns; adjacent columns complete the power array [6].

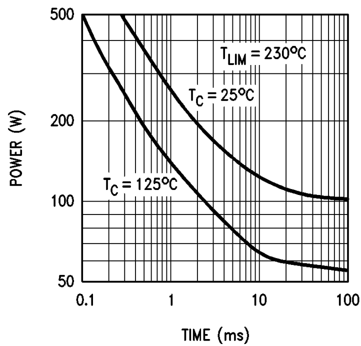

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Figure 10. This graph gives the pulse power required to activate dynamic safe-area protection in the time indicated. The curves suggest that there is no important response time limitation.

The transient response of dynamic safe-area protection under adverse conditions is shown in *Figure 11*. Peak dissipation before limit is 900W, about ten times the continuous rating. Even so, the protection circuitry detects the fault and effects shutdown in 150 µs. The control circuitry is less stable in limit at lower fault voltages under certain circumstances. There can be considerably more ringing or oscillations in limit.

When compared to conventional methods, the worst-case, guaranteed ratings of dynamic safe-area protection are most impressive in that they do not differ greatly from the

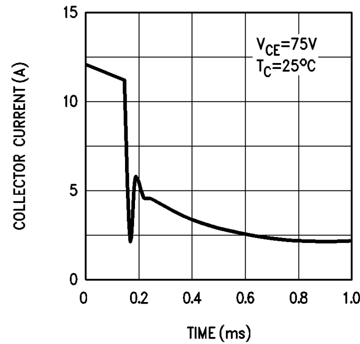

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Figure 11. The transient response of dynamic safe-area protection to a gross overload demonstrates the effectiveness of the method [6].

typicals. This is illustrated by the safe-area curve in *Figure 12*. This curve can be guaranteed in that it represents the production distribution with the exception of die-attach voids that can be eliminated by good workmanship. It should be noted that power ratings on this curve are limited by a maximum junction temperature of 200°C, not the 225°C thermal-limit temperature.

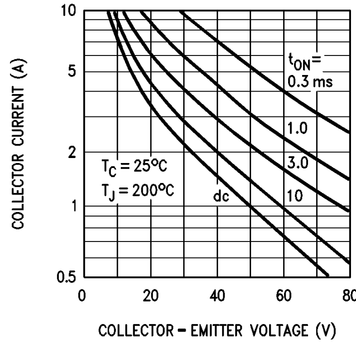

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Figure 12. Guaranteed specifications with dynamic safe-area protection are not much different from typical. This illustrates that tolerance problems of conventional techniques can be avoided.

Dynamic safe-area protection with its peak temperature limiting has the advantage that parts can be 100-percent tested into thermal limit, giving a quantative measure of thermal resistance. This differs from conventional techniques where questionable indirect methods are used.

applications

Dynamic safe-area protection can be considered revolutionary in that it extends the power capability of monolithic IC's by more than an order of magnitude in certain cases. However, there is a penalty of increased complexity that may not pay off in all cases. In order to develop an appreciation for the method, it is necessary to compare it critically with conventional techniques.

Conventional protection uses foldback current limiting to match the dc safe-area curve of the power transistor. In practice, the limiting current has been subject to a 2:1 tolerance, minimum to maximum, in the production distribution at 15V. At 30V, the tolerance buildup is 5:1; at 50V it is 8:1. These tolerances must be inferred from manufacturer's data sheets. Specifying min/max limits at 15V are not common; hard specifications at higher voltages are rare. When specified, limits are as stated. Worst-case design cannot take advantage of more than the minimum but must allow for the maximum with an overload.

Figure 13 plots the junction temperature rise of a power transistor as a function of case temperature in an IC using conventional protection. Thermal limit temperature is 150°C at a location on the die that is sensitive to one-third the internal temperature rise of the power transistor. Foldback current limit is assumed to limit temperature rise to 150°C.

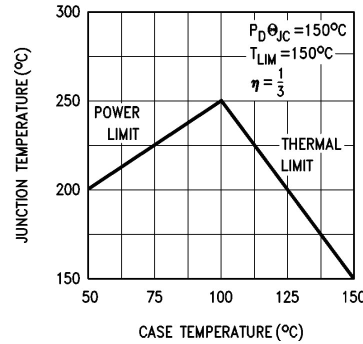

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Figure 13. Power transistor junction temperature as a function of case temperature where the thermal sensor responds to one-third the temperature rise. Factors not considered can cause the temperature to peak at a much higher value.

When there is little heat removal by a heat sink, the case temperature will nearly equal the steady-state, peak-junction temperature. In this case, junction temperature will be limited near the 150°C thermal limit temperature. As heat sinking is provided, however, the power transistor must be enough hotter than the thermal sensor to support the resulting thermal gradients. Junction temperature in the power transistor will rise with decreasing case temperature in thermal limit until the power-limit curve is intersected. The worst case junction temperature in limit is given by

$$T_{MAX} = T_{LIM} + [1 - \eta]\, \theta_{JC} P_D,$$

where T_{LIM} is the thermal limit temperature, η is the fraction of the junction temperature rise seen by the thermal-limit sensor, θ_{JC} is the thermal resistance of the power transistor and P_D the power dissipation with the maximum value of current limit.

The plot in *Figure 13* is representative of many power ICs for typical operating conditions. Power limiting at the high end of the production distribution will increase the worst-case temperature well above 250°C. Further, thermal destabilization in the secondary-breakdown-limited portion of the safe-area curve can drastically alter results.

Clearly, the advantage of dynamic safe-area protection is that it maximizes the dissipation rating of a power transistor, particularly at higher voltages and under pulse conditions. Not all applications require this sophistication. A 5V regulator for logic supplies is an example. The series pass transistor must be made large to obtain low saturation voltage at high current. The resulting thermal resistance is low enough that power dissipation capability is not a limiting factor, and conventional protection can give satisfactory results.

With higher voltage regulators, however, conventional protection may not provide enough short-circuit current to bring up the load under worst-case conditions. Dynamic safe-area protection can provide much more start-up current.

High voltage, class-B power amplifiers can take full advantage of dynamic safe-area protection. They are frequently called upon to drive reactive loadlines where peak dissipation can occur at levels approaching the total supply voltage. Further, the peak dissipation can be several times the average. In this kind of service, dynamic safe-area protection can deliver ten times the output power for a given die size when compared to conventional methods. In the example cited earlier, the protection circuitry, although complex, takes up about 10-percent of the die area.

Dynamic safe-area protection is not necessarily limited to IC applications. Discrete power transistors can be provided with an internal, distributed temperature sensor. Thermal limiting would then be provided by external circuitry.

conclusions

A new protection system has been developed for power transistors that allows use of their full capabilities as manufactured, rather than those established by a hypothetical safe-area curve. As a result, higher power ratings can be *guaranteed* with a given die size. At the same time, reliability is improved by controlling peak temperature and by permitting individual devices to be 100-percent tested for rated power.

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